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In re Application of: GEOFFREY S. STRONGIN DALE E. GULICK	Examiner: X. THAI
Serial No.: 09/853,335	Group Art Unit: 2111
Filed: May 11, 2001	Att'y Docket: 2000.063200
For: ASSET SHARING BETWEEN HOST PROCESSOR AND SECURITY HARDWARE	Customer No. 23720

APPEAL BRIEF

CERTIFICATE OF MAILING
37 C.F.R. 1.8

I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date below:

7.26.05 (Date)

Kathryn Dana (Signature)

MS APPEAL BRIEF - PATENT
Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant hereby submits this revised Appeal Brief to the Board of Patent Appeals and Interferences in response to the Notice of Non-Compliant Appeal Brief dated July 14, 2005. The one-month date for reply is August 14, 2005.

No fees are believed due for this revised Appeal Brief. However the Commissioner is authorized to deduct any required fees from **Advanced Micro Devices, Inc.'s Deposit Account 01-0365/TT4207.** In the event the monies in that account are insufficient, the Commissioner is authorized to withdraw funds from Williams, Morgan & Amerson, P.C. Deposit Account No. **50-0786/2000.063200/TT4207**.

I. REAL PARTY IN INTEREST

The present application is owned by Advanced Micro Devices, Inc. The assignment of the present application to Advanced Micro Devices, Inc., is recorded at Reel 11808, Frame 0515.

II. RELATED APPEALS AND INTERFERENCES

Applicant is not aware of any related appeals and/or interferences that might affect the outcome of this proceeding.

III. STATUS OF CLAIMS

Claims 1-13 and 15-57 are pending in the application. The claims as currently pending are attached as Appendix A. Claims 1-2, 4-8, 10-13, 15, and 30-57 stand rejected under 35 U.S.C. § 102(e) as allegedly being anticipated by Moriarty, et al (U.S. Patent No. 6,446,149). Claims 1-2, 4-8, 10-13, 15, 30-31, and 47-48 stand rejected under 35 U.S.C. § 102(e) as allegedly being anticipated by Parks (U.S. Patent No. 6,356,983). Claims 1-13, 15, and 30-57 stand rejected under 35 U.S.C. § 102(e) as allegedly being anticipated by Scholhamer, et al (U.S. Patent No. 6,636,921). Claims 16-19 and 21-29 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Moriarty in view of Kao, et al (U.S. Patent No. 6,651,168).

IV. STATUS OF AMENDMENTS

There were no amendments after the final rejections.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Many personal computers use an x86 operating system to implement an x86 operating environment. From a hardware point of view, an x86 operating environment provides little for protecting user privacy, providing security for corporate secrets and assets, or protecting the ownership rights of content providers. All of these goals, privacy, security, and ownership (collectively, PSO) are becoming critical in an age of Internet-connected computers. The original personal computers were not designed in anticipation of PSO needs. From a software point of view, the x86 operating environment is equally poor for PSO. The ease of direct access to the hardware through software or simply by opening the cover of the personal computer allows an intruder or thief to compromise most security software and devices. The personal computer's exemplary ease of use only adds to the problems for PSO.

At least in part to address some of the PSO needs of Internet-connected computers, the present invention provides a bus interface logic. As set forth in independent claims 1, 7, 18, 30, 41, 42, and 47, various embodiments of the bus interface logic include a storage location configured to store a master mode bit. The bus interface logic is configured to exchange data only with a device that caused the master mode bit to be set when the master mode bit is set. As defined in the specification, a master mode bit is a bit that indicates that one or more bus interface logics or other devices will be used to establish a secure transmission channel between a master mode logic and a data input device while operating outside the operating system.

Exemplary embodiments of bus interface logics include the bus interface logics 134B, 134C, 134D, and 134E of south bridge 330F. The bus interface logics 134B, 134C, 134D, and 134E include IDE interface logic 134B, USB interface logic 134C, LPC bus interface logic 134D, and SMBus bus interface logic 134E, respectively. Each bus interface logic 134B, 134C,

134D, and 134E include a master mode register 4799 including a master mode bit (not shown in Figure 36). Secure input devices may include the USB hub 315, the biometric device 320, and the smart card reader 325. See, *e.g.*, Patent Application, page 93, ll. 23-24 and page 94, line 2 – page 96, line 8, as well as Figures 36 and 37.

Master mode operations of the computer subsystem 4700 may advantageously allow for secure input of data, such as biometric data or smart card data provided by the biometric device 320 and/or the smart card reader 325, without the unencrypted data being accessible to the operating system. Master mode creates a secure communications channel between the master mode logic 4790 and the data input device. Thus, master mode operation may advantageously allow for user authentication, such as via the biometric device 320 and/or the smart card reader 325, without the operating system or a program running under the operating system snooping on the authentication data stream. See, *e.g.*, Patent Application, page 93, ll. 23-24 and page 94, line 2 – page 96, line 8, as well as Figures 36 and 37.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Appellant respectfully requests that the Board review and overturn the four rejections present in this case. The following issues are presented on appeal in this case:

(A) Whether claims 1-2, 4-8, 10-13, 15, and 30-57 are anticipated by Moriarty;

(B) Whether claims 1-2, 4-8, 10-13, 15, 30-31, and 47-48 are anticipated by Parks;

(C) Whether claims 1-13, 15, and 30-57 are anticipated by Scholhamer; and

(D) Whether claims 16-19 and 21-29 are obvious over Moriarty in view of Kao.

VII. ARGUMENT

A. Claims 1-2, 4-8, 10-13, 15, and 30-57 are not anticipated by Moriarty.

An anticipating reference by definition must disclose every limitation of the rejected claim in the same relationship to one another as set forth in the claim. *In re Bond*, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). Furthermore, an inventor may act as his or her own lexicographer. See MPEP, §2111.01.

Moriarty describes allowing exclusive access by a bus master to a shared critical resource based upon the contents of a semaphore memory cell. However, Moriarty does not describe or suggest a master mode bit, *i.e.* a bit that indicates that one or more bus interface logics or other devices will be used to establish a secure transmission channel between a master mode logic and a data input device while operating outside the operating system, as defined in the Patent Application.

In the Final Office Action, the Examiner alleges that the features upon which Appellant relies are not recited in the rejected claims. Appellant respectfully disagrees. Independent claims 1, 7, 18, 30, 41, 42, and 47 set forth a master mode bit. Moreover, Appellant has clearly defined the term, "master mode bit," as a bit that indicates that one or more bus interface logics or other devices will be used to establish a secure transmission channel between a master mode logic and a data input device while operating outside the operating system. See, *e.g.*, Patent Application, page 93, ll. 23-24 and page 94, line 2 – page 96, line 8, as well as Figures 36 and 37.

For at least the aforementioned reasons, Appellants respectfully submit that Moriarty fails to disclose every limitation of the rejected claim in the same relationship to one another as set forth in the claim. In particular, Moriarty fails to describe a master mode bit. Thus, Appellants submit that claims 1-2, 4-8, 10-13, 15, and 30-57 are not anticipated by Moriarty.

B. Claims 1-2, 4-8, 10-13, 15, 30-31, and 47-48 are not anticipated by Parks.

Parks describes techniques for providing cache coherency and/or atomic transactions. However, Park does not describe or suggest a master mode bit, *i.e.* a bit that indicates that one or more bus interface logics or other devices will be used to establish a secure transmission channel between a master mode logic and a data input device while operating outside the operating system, as defined in the Patent Application.

In the Final Office Action, the Examiner alleges that the features upon which Appellant relies are not recited in the rejected claims. Appellant respectfully disagrees. Independent claims 1, 7, 18, 30, 41, 42, and 47 set forth a master mode bit. Moreover, Appellant has clearly defined the term, "master mode bit," as a bit that indicates that one or more bus interface logics or other devices will be used to establish a secure transmission channel between a master mode logic and a data input device while operating outside the operating system. See, *e.g.*, Patent Application, page 93, ll. 23-24 and page 94, line 2 – page 96, line 8, as well as Figures 36 and 37.

For at least the aforementioned reasons, Appellants respectfully submit that Park fails to disclose every limitation of the rejected claim in the same relationship to one another as set forth in the claim. In particular, Park fails to describe a master mode bit. Thus, Appellants submit that claims 1-2, 4-8, 10-13, 15, 30-31, and 47-48 are not anticipated by Parks.

C. Claims 1-13, 15, and 30-57 are not anticipated by Scholhamer.

Scholhamer describes a SCSI bus repeater circuit that isolates one or more devices on a terminated SCSI bus segment. However, Scholhamer does not describe or suggest a master mode bit, *i.e.* a bit that indicates that one or more bus interface logics or other devices will be used to

establish a secure transmission channel between a master mode logic and a data input device while operating outside the operating system, as defined in the Patent Application.

In the Final Office Action, the Examiner alleges that the features upon which Appellant relies are not recited in the rejected claims. Appellant respectfully disagrees. Independent claims 1, 7, 18, 30, 41, 42, and 47 set forth a master mode bit. Moreover, Appellant has clearly defined the term, "master mode bit," as a bit that indicates that one or more bus interface logics or other devices will be used to establish a secure transmission channel between a master mode logic and a data input device while operating outside the operating system. See, *e.g.*, Patent Application, page 93, ll. 23-24 and page 94, line 2 – page 96, line 8, as well as Figures 36 and 37.

For at least the aforementioned reasons, Appellants respectfully submit that Scholhamer fails to disclose every limitation of the rejected claim in the same relationship to one another as set forth in the claim. In particular, Scholhamer fails to describe a master mode bit. Thus, Appellants submit that claims 1-13, 15, and 30-57 are not anticipated by Scholhamer.

D. Claims 16-19 and 21-29 are not obvious over Moriarty in view of Kao.

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (CCPA 1974). Second, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. That is, there must be something in the prior art as a whole to suggest the desirability, and thus the obviousness, of making the combination. *Panduit Corp. v. Dennison Mfg. Co.*, 810 F.2d 1561 (Fed. Cir. 1986). In fact, the absence of a suggestion to combine is dispositive in an

obviousness determination. *Gambro Lundia AB v. Baxter Healthcare Corp.*, 110 F.3d 1573 (Fed. Cir. 1997). The mere fact that the prior art can be combined or modified does not make the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 U.S.P.Q.2d 1430 (Fed. Cir. 1990); M.P.E.P. § 2143.01. Third, there must be a reasonable expectation of success. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991); M.P.E.P. § 2142.

As discussed above, Moriarty fails to describe or suggest a master mode bit. Moreover, Moriarty is completely silent with regard to operating in a master mode, and so Moriarty provides no suggestion or motivation to modify the prior art to arrive at Appellants claimed invention. The Examiner relies upon Kao to describe an authentication framework. However, Kao fails to remedy the aforementioned fundamental deficiency of the primary reference. Thus, Appellants respectfully submit that claims 16-19 and 21-29 are not obvious over Moriarty in view of Kao.

XIII. CONCLUSION

In view of the foregoing, it is respectfully submitted that the Examiner erred in not allowing all claims pending in the present application, claims 1-13 and 15-57, over the prior art of record. The undersigned may be contacted at (713) 934-4052 with respect to any questions, comments or suggestions relating to this appeal.

Respectfully submitted,

Date: 7/26/05

Mark W. Sincell, Ph.D.
Reg. No. 52,226
WILLIAMS, MORGAN & AMERSON
10333 Richmond, Suite 1100
Houston, Texas 77042
(713) 934-7000
(713) 934-7011 (facsimile)

AGENT FOR APPLICANTS

CLAIMS APPENDIX

1. (Original) A bus interface logic configured with a storage location configured to store a master mode bit, wherein the bus interface logic is configured to exchange data only with a master device that caused the master mode bit to be set when the master mode bit is set.

2. (Original) The bus interface logic of claim 1 further configured to flush output buffers in response to the master mode bit being reset.

3. (Previously Presented) The bus interface logic of claim 1 further configured to operate within the operating system after the master mode bit is reset.

4. (Original) The bus interface logic of claim 1, wherein the storage location is further configured to store one or more addresses, and wherein the bus interface logic is configured to exchange data only with the one or more addresses.

5. (Original) The bus interface logic of claim 4, wherein the one or more addresses comprise an address range, wherein the bus interface logic is configured to exchange data only within the address range.

6. (Original) The bus interface logic of claim 1, wherein the storage location is further configured to store one or more addresses, and wherein the bus interface logic is configured not to exchange data with the one or more addresses.

7. (Original) A computer system, comprising:

a master device configured to set and reset a master mode bit; and

one or more bus interface logics, each configured with a storage location configured to store the master mode bit, wherein the bus interface logics are configured to exchange data only with the master device when the master mode bit is set.

8. (Original) The computer system of claim 7, wherein the bus interface logics are further configured to flush output buffers in response to the master mode bit being reset.

9. (Previously Presented) The computer system of claim 7, wherein the one or more bus interface logics are further configured to operate within the operating system after the master mode bit is reset.

10. (Original) The computer system of claim 7, wherein the storage location is further configured to store one or more addresses, and wherein the one or more bus interface logics are configured to exchange data only with the one or more addresses.

11. (Original) The computer system of claim 10, wherein the one or more addresses comprise an address range, wherein the one or more bus interface logics are configured to exchange data only within the address range.

12. (Original) The computer system of claim 10, wherein the master device is further configured to store the one or more addresses in the storage location along with the master mode bit.

13. (Previously Presented) The computer system of claim 7, wherein the storage location is further configured to store one or more addresses, and wherein the one or more bus interface logic are configured not to exchange data with the one or more addresses when in the master mode.

14. (Cancelled)

15. (Original) The computer system of claim 7, further comprising:

a processor configured to exchange data through the one or more bus interface logics when the master mode bit is not set; and

wherein the one or more bus interface logics are further configured not to exchange data for the processor when the master mode bit is set.

16. (Original) The computer system of claim 7, wherein the master device comprises a crypto-processor.

17. (Original) The computer system of claim 7, wherein the master device comprises security hardware.

18. (Original) A computer system, comprising:

a master device;

a device, different from the master device, configured to provide authentication data to the master device;

at least a first bus interface logic coupled to the master device, wherein the first bus interface logic comprises a first storage location for storing a first master mode bit; and

at least a second bus interface logic coupled to the device, wherein the first bus interface logic comprises a second storage location for storing a second master mode bit;

wherein the master device is configured to cause to be set the first master mode bit in the first storage location and the second master mode bit in the second storage location;

wherein the first bus interface logic is configured to exchange data only between the master device and the second bus interface logic when the first master mode bit is set; and

wherein the second bus interface logic is configured to exchange data only between the device and the first bus interface logic when the second master mode bit is set.

19. (Original) The computer system of claim 18, wherein the master device is configured to set and reset the first and second master mode bits.

20. (Original) The computer system of claim 18, wherein the first and second bus interface logics are further configured to flush output buffers in response, respectively, to the first and second master mode bits being reset.

21. (Previously Presented) The computer system of claim 18, wherein the first and second bus interface logics are further configured, respectively, to operate within the operating system after the first and second master mode bits are reset.

22. (Original) The computer system of claim 18, wherein the first and second storage locations are further each configured to store one or more addresses, and wherein the first and second bus interface logics are configured, respectively, to exchange data only with the one or more addresses as stored therein.

23. (Original) The computer system of claim 22, wherein the one or more addresses comprise an address range, wherein the first and second bus interface logics are configured to exchange data only within the address range.

24. (Original) The computer system of claim 22, wherein the master device is further configured to store the one or more addresses in the first and second storage locations along with the first and second master mode bits.

25. (Original) The computer system of claim 18, wherein the first and second storage locations are further configured to store one or more addresses, and wherein the first and second bus interface logics are each configured not to exchange data with the one or more addresses stored therein.

26. (Original) The computer system of claim 22, wherein the master device is further configured to store the one or more addresses in the first and second storage locations along with the first and second master mode bits.

27. (Original) The computer system of claim 18, further comprising:

a processor configured to exchange data through the first and second bus interface logics when the first and second master mode bits are not set; and

wherein the first and second bus interface logics are each further configured not to exchange data for the processor when the first and second master mode bits, respectively, are set.

28. (Original) The computer system of claim 18, wherein the master device comprises a crypto-processor.

29. (Original) The computer system of claim 18, wherein the master device comprises security hardware.

30. (Original) A method of operating a computer system, the method comprising:

setting a master mode bit for a bus interface logic;

passing a data request through the bus interface logic only for a specified device;

receiving data in response to the data request from the specified device; and

resetting the master mode bit.

31. (Original) The method of claim 30, further comprising:

setting a master mode bit in another bus interface logic; and

passing the data request from the another bus interface logic to the bus interface logic in only for the specified device.

32. (Original) The method of claim 30, wherein setting a master mode bit for a bus interface logic comprises a master device setting the master mode bit for the bus interface logic; and wherein passing the data request through the bus interface logic only for the specified device further comprises the master device providing the data request through the bus interface logic only for the specified device.

33. (Original) The method of claim 30, further comprising:

making an attempt to access the bus interface logic; and

rejecting the attempt to access the bus interface logic by other than the master device or the specified device, when the master mode bit is set.

34. (Original) The method of claim 30, further comprising:

resetting the master mode bit; and

flushing buffers of the bus interface logic in response to resetting the master mode bit.

35. (Original) The method of claim 34, further comprising:

making an attempt to access the bus interface logic; and

accessing the bus interface logic in response to making the attempt to access the bus interface logic by other than the master device or the specified device, after the master mode bit is reset.

36. (Original) The method of claim 30, further comprising:

storing one or more address locations along with the master mode bit for the bus interface logic.

37. (Original) The method of claim 36, further comprising:

restricting data transmissions only to the one or more address locations.

38. (Original) The method of claim 36, further comprising:

restricting data transmissions only to within an address range defined by the one or more address locations.

39. (Original) The method of claim 36, further comprising:

restricting data transmissions from the one or more address locations.

40. (Original) The method of claim 36, further comprising:

restricting data transmissions from within an address range defined by the one or more address locations.

41. (Original) A computer system, comprising:

means for storing an indicator of a master mode;

means for restricting data transfers when the indicator of the master mode is set;

means for resetting the indicator of the master mode.

42. (Original) A computer system, comprising:

means for setting a master mode bit for a bus interface logic;

means for passing a data request through the bus interface logic only for a specified device;

means for receiving data in response to the data request from the specified device; and

means for resetting the master mode bit.

43. (Original) The computer system of claim 42, further comprising:

means for setting a master mode bit in another bus interface logic; and

means for passing the data request from the another bus interface logic to the bus interface logic only for the specified device.

44. (Original) The computer system of claim 42, further comprising:

means for rejecting an attempt to access the bus interface logic by other than the master device or the specified device, when the master mode bit is set.

45. (Original) The computer system of claim 42, further comprising:

means for resetting the master mode bit; and

means for flushing buffers of the bus interface logic in response to resetting the master mode bit.

46. (Original) The computer system of claim 45, further comprising:

means for accessing the bus interface logic in response to making an attempt to access the bus interface logic by other than the master device or the specified device, after the master mode bit is reset.

47. (Original) A computer readable program storage device encoded with instructions that, when executed by a computer, performs a method of operating a computer system, the method comprising:

setting a master mode bit for a bus interface logic;

passing a data request through the bus interface logic only for a specified device;

receiving data in response to the data request from the specified device; and

resetting the master mode bit.

48. (Original) The computer readable program storage device of claim 47, the method further comprising:

setting a master mode bit in another bus interface logic; and

passing the data request from the another bus interface logic to the bus interface logic only for the specified device.

49. (Original) The computer readable program storage device of claim 47, wherein setting a master mode bit for a bus interface logic comprises a master device setting the master mode bit for the bus interface logic; and wherein passing the data request through the bus interface logic only for the specified device further comprises the master device providing the data request through the bus interface logic only for the specified device.

50. (Original) The computer readable program storage device of claim 47, the method further comprising:

making an attempt to access the bus interface logic; and

rejecting the attempt to access the bus interface logic by other than the master device or the specified device, when the master mode bit is set.

51. (Original) The computer readable program storage device of claim 47, the method further comprising:

resetting the master mode bit; and

flushing buffers of the bus interface logic in response to resetting the master mode bit.

52. (Original) The computer readable program storage device of claim 51, the method further comprising:

making an attempt to access the bus interface logic; and

accessing the bus interface logic in response to making the attempt to access the bus interface logic by other than the master device or the specified device, after the master mode bit is reset.

53. (Original) The computer readable program storage device of claim 47, the method further comprising:

storing one or more address locations along with the master mode bit for the bus interface logic.

54. (Original) The computer readable program storage device of claim 53, the method further comprising:

restricting data transmissions only to the one or more address locations.

55. (Original) The computer readable program storage device of claim 53, the method further comprising:

restricting data transmissions only to within an address range defined by the one or more address locations.

56. (Original) The computer readable program storage device of claim 53, the method further comprising:

restricting data transmissions from the one or more address locations.

57. (Original) The computer readable program storage device of claim 53, the method further comprising:

restricting data transmissions from within an address range defined by the one or more address locations.